	Application No.	Applicant(s)
Notice of Allowability	10/517,056	NAKABE, FUTOSHI
	Examiner	Art Unit
	Kimberly D. Nguyen	2876
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. X This communication is responsive to communication filed June 9, 2006.		
2. The allowed claim(s) is/are 1-8.		
3.		
attached Examiner's comment regarding REQUIREMENT  Attachment(s)  1. Notice of References Cited (PTO-892)  2. Notice of Draftperson's Patent Drawing Review (PTO-948)  3. Information Disclosure Statements (PTO-1449 or PTO/SB/Paper No./Mail Date	5. Notice of Informal 6. Interview Summary Paper No./Mail Da 708), 7. Examiner's Amend	Patent Application (PTO-152) y (PTO-413), ate

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## **DETAILED ACTION**

## Amendment

1. Acknowledgment is made of Amendment filed June 9, 2006.

## Allowable Subject Matter

- 2. Claims 1-8 are allowed.
- 3. The following is an examiner's statement of reasons for allowance:

Iijima (US 5,293,029) teaches an IC card 1 comprises, among other things/elements, a random number generator 5 for generating random number data.

Fujioka (US 6,480,869) teaches a non-contact IC card having a single random-number generating circuit 107 as shown in figure 3. The random-number generating circuit comprising a plurality of shift registers synchronized with a clock and cascaded together, a circuit that obtains the sum of the outputs of more than one of the shift registers and inputs the obtained sum to the input terminal of the shift register on the first level, and a clock generating circuit that inputs a clock signal to each of the shift registers. One or more of the shift registers have external-signal input terminals and an addition circuit that adds bit data input through the external-signal input terminals to bit data of one or more of the bits stored within. The random-number generating circuit outputs as random-number data the bit data obtained from the addition by the addition circuit.

Fujioka (US 6,040,786) teaches a non-contact IC card 200 having a single random-number generating circuit 207, as shown in figure 2, that is used for determining the timing of transmitting a response signal in answering a second or later polling trial by reader/writer 100.

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However, Iijima, Fujioka '869, Fujioka '786, taken alone or in combination thereof, fails to teach or fairly suggest a contact-less IC card that is configured to execute a plurality of applications and responds to a request from a reader/writer using a slot that was set by a random number, wherein the contact-less IC card comprising a plurality of random-number-generation units that are separate from the applications, and operable to independently generate a random number for setting the slot; a random-number-generation-instruction unit operable to designate the random-number-generation unit to be used for a response to the request from among the plurality of random-number-generation units; and a slot-setting unit operable to use the random number generated by the random-number-generation unit that was designated by the random-number-generation-instruction unit and perform the response.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

## Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly D. Nguyen whose telephone number is 571-272-2402. The examiner can normally be reached on Monday-Friday 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on 571-272-2398. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lin Mguyen

August 18, 2006